INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/86	Serial No. 10/501,845
	Applicant(s) Vorbach et al.	
	Filing Date August 26, 2005	Group Art Unit 2183

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	7,028,107	April 11, 2006	Vorbach et al.			
	7,595,659	September 29, 2009	Vorbach et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Altera, "APEX 20K Programmable Logic Device Family," Altera Corporation Data Sheet, March 2004, ver. 5.1, pp. 1-117.
	XILINX, "Virtex-E 1.8 V Extended Memory Field Programmable Gate Arrays," (v2.2) September 10, 2002, Xilinx Production Product Specification, pp. 1-52.
	XILINX, "Virtex-II and Virtex-II Pro X FPGA Platform FPGAs: Complete Data Sheet," (v4.6) March 5, 2007, pp. 1-302.
	XILINX, "Virtex-II Platform FPGAs: Complete Data Sheet," (v3.5) November 5, 2007, pp. 1-226.

EXAMINER	/Keith Vicary/	DATE CONSIDERED	02/25/2010

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /KV/